

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A wafer of monocrystalline semiconductor material, comprising at least one buried cavity having a wall completely surrounded by said monocrystalline material, the cavity wall coated ~~and covered with~~ a layer of material inhibiting epitaxial growth.

2. (Canceled)

3. (Previously Presented) The wafer of claim 1 wherein said material inhibiting epitaxial growth comprises oxide.

4. (Previously Presented) The wafer of claim 1 wherein said material inhibiting epitaxial growth comprises TEOS.

5. (Previously Presented) The wafer of claim 1 wherein said material inhibiting epitaxial growth comprises nitride.

6. (Original) The wafer of claim 1, further comprising a plurality of buried channels adjacent and separated from each other by dividers.

7. (Original) The wafer of claim 1, further comprising a plurality of buried cavities at different heights.

8. (Original) A structure formed in a substrate of semiconductor material, the structure comprising:

at least one trench formed in the substrate, the at least one trench having an open top and an open bottom, and a coating on the lateral walls of the at least one trench with material resistant to etching;

a cavity having walls formed below each at least one trench and in communication with the open bottom of the at least one trench, and a coating on the walls of the cavity with material inhibiting epitaxial growth; and

an epitaxial layer formed on the substrate to cover the open top of the at least one trench and to encase the at least one trench and the cavity in the substrate.

9. (Original) The structure of claim 8, comprising a plurality of trench and cavity pairs formed in the substrate.

10. (Original) The structure of claim 9, wherein each trench and cavity pair are formed at different levels within the substrate.

11. (Original) The structure of claim 9, wherein each trench and cavity pair are formed to have different cross-sectional configurations.

12. (Original) The structure of claim 9, wherein each trench and cavity pair are formed to have different cross-sectional sizes.

13. (Original) The structure of claim 9, wherein each trench and cavity pair are formed to have a different cross-sectional size and to be formed at different levels in the substrate.

14. (Original) A wafer of semiconductor material, comprising:
a buried cavity formed in the semiconductor material having an open top, the cavity coated with a material inhibiting epitaxial growth; and
a membrane formed on the substrate to cover the open top of the cavity to encase the cavity in the substrate.

15. (Original) A wafer of semiconductor material, comprising:
a plurality of buried cavities formed in and completely surrounded by the semiconductor material, each cavity of the plurality of buried cavities coated with a layer of material inhibiting epitaxial growth.

16. (Original) The wafer of claim 15, wherein each cavity of the plurality of buried cavities are formed parallel to one another and at a right angle with respect to a drawing plane of the semiconductor material.

17. (Original) The wafer of claim 16, wherein the plurality of cavities are formed at the same height.

18. (Original) The wafer of claim 16, wherein each of the cavities of the plurality of cavities are formed at a different level in the semiconductor material.

19. (Previously Presented) A structure formed in semiconductor material, the structure comprising:

a cavity formed in the semiconductor material and having an open top; and
a membrane formed of epitaxial growth on the semiconductor material that covers the open top of the cavity in the substrate, the membrane having a thickness in the range of between 1 and 3 μm .

20. (Canceled)

21. (Previously Presented) The structure of claim 19, further comprising at least one trench etched into the membrane and of a depth to be in communication with the cavity.

22. (Previously Presented) The wafer of claim 14, wherein the membrane has a thickness in the range of between 1 and 3 μm .

23. (Previously Presented) The wafer of claim 14, further comprising at least one trench etched into the membrane and of a depth to be in communication with the cavity.

24. (Previously Presented) The wafer of claim 14, wherein the material inhibiting epitaxial growth comprises TEOS.

25. (Previously Presented) The wafer of claim 14, wherein the material inhibiting epitaxial growth comprises oxide.

26. (Previously Presented) The wafer of claim 14, wherein the material inhibiting epitaxial growth comprises nitride.

27. (Previously Presented) The wafer of claim 14, further comprising a plurality of buried channels adjacent and separated from each other by dividers.

28. (New) A wafer of monocrystalline semiconductor material, comprising at least one buried cavity completely surrounded by said monocrystalline material and covered with a layer of material inhibiting epitaxial growth; and

a plurality of buried channels adjacent and separated from each other by dividers.

29. (New) The wafer of claim 28, wherein the material inhibiting epitaxial growth comprises oxide.

30. (New) The wafer of claim 28, wherein the material inhibiting epitaxial growth comprises TEOS.

31. (New) The wafer of 28, wherein the material inhibiting epitaxial growth comprises nitride.

32. (New) A wafer of monocrystalline semiconductor material, comprising at least one buried cavity completely surrounded by said monocrystalline material and covered with a layer of material inhibiting epitaxial growth; and

a plurality of buried cavities at different heights within the wafer of monocrystalline semiconductor material.

33. (New) The wafer of claim 32, wherein the material inhibiting epitaxial growth comprises oxide.

34. (New) The wafer of claim 32, wherein the material inhibiting epitaxial growth comprises TEOS.

35. (New) The wafer of 32, wherein the material inhibiting epitaxial growth comprises nitride.